WHAT IS CLAIMED IS:

1	1.	A method of self-programming a graphics processing unit (GPU), the			
2	method comprising:				
3	rece	eiving from the CPU a blit instruction defining a blit operation; and			
4	stor	ring a first control value in a control register using the blit operation,			
5	wherein the first co	ontrol value in the control register determines the behavior of the GPU.			
1	2.	The method of claim 1, further comprising applying the blit operation			
2	to a second control value to determine the first control value.				
1	3.	The method of claim 2, wherein the second control value is stored in a			
2	memory.				
1	4.	The method of claim 3, wherein the memory is a second control			
2	register.				
1	5.	The method of claim 3, wherein the second control value is stored in a			
2	table of control values accessed by an index value.				
1	6.	The method of claim 5, further comprising changing the index value to			
2	access a third control	value in the table following the blit operation.			
1	7.	The method of claim 2, wherein the second control value is a starting			
2	memory address for a	display buffer.			
1	8.	The method of claim 2, wherein the second control value is a clip plane			
2	distance.				
1	9.	The method of claim 8, wherein the second control value is greater			
2	than the depth extent of an object.				
1	10.	The method of claim 1, wherein the blit operation includes a colorkey			
2	operation.				
1	11.	The method of claim 1, wherein the blit operation includes a logic			
2	operation on the first control value.				

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1	12. The method of claim 1, wherein the blit operation includes a pattern			
2	copy operation.			
1	13. The method of claim 2, wherein the first control value is a copy of the			
2	second control value.			
1	14. The method of claim 1, wherein receiving comprises reading a blit			
2	instruction from a command buffer asynchronously with the CPU.			
1	15. A graphics rendering system comprising:			
2	a central processing unit;			
3	a graphics processing unit adapted to create graphics data in response to a			
4	graphics command, wherein the graphics processing unit has a control register and a blit			
5	engine; and			
6	a command buffer adapted to receive at least a first graphics command			
7	from the central processing unit and further adapted to communicate the first graphics			
8	command to the graphics processing unit;			
9	wherein, the blit engine is adapted to store a first control value in the			
10	control register in response to the first graphics command.			
1	16. The graphics rendering system of claim 15, wherein the blit engine is			
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1	17. The graphics rendering system of claim 16, further comprising a			
2	memory adapted to store the second control value.			
1	18. The graphics rendering system of claim 17, wherein the memory is a			
2	second control register.			
1	19. The graphics rendering system of claim 17, wherein the memory			
2	comprises a table of control values including the second control value and accessed by an			
3	index value.			
1	20. The graphics rendering system of 16, wherein the second control value			
2	is a starting memory address for a display buffer.			

1		21.	The graphics rendering system of claim 16, wherein the second control	
2	value is a clip plane distance.			
1		22.	The graphics rendering system of claim 16, wherein the blit engine is	
2	adapted to per	form a	colorkey operation on the second control value.	
1		23.	The graphics rendering system of claim 15, wherein the blit engine is	
2	adapted to perform a logic operation on the first control value.			
1		24.	A method of self-programming a graphics processing unit (GPU) using	
2	a set of GPU commands created by a driver, the method comprising:			
3		writing	g a first set of rendering commands to a command buffer;	
4	writing a set of self-programming commands including a blit instruction to the			
5	command buffer; and			
6		writing	g a second set of rendering commands to the command buffer.	
1		25.	The method of claim 24, wherein the first set of rendering commands,	
2	the set of self-	progran	nming commands, and the second set of rendering commands are	
3	written sequen	tially to	the command buffer.	
1		26.	The method of claim 24, wherein the first set of rendering commands	
2	is associated w	ith a fir	rst image to be rendered to a first display buffer, the second set of	
3	rendering commands is associated with a second image to be rendered to a second display			
4	buffer, and the	set of s	self-programming commands is adapted to instruct the GPU to display	
5	the first image			
1		27.	The method of claim 26, wherein the blit instruction is adapted to store	
2	a memory add	ress ass	sociated with the first display buffer in a control register of the GPU.	
1		28.	The method of claim 24, wherein the first set of rendering commands	
2	is associated w	vith a bo	ounding box associated with an object and the second set of rendering	
3	commands is associated with the object; and further wherein the set of self-programming			

commands is adapted to instruct the GPU to evaluate the visibility of the bounding box and to

optionally bypass the rendering of the object in response to the evaluation of the visibility of

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the bounding box.

1	29	9.	The method of claim 28, wherein the blit instruction includes a
2	colorkey operation on a register of the GPU.		
1	30	0.	The method of claim 29, wherein the register of the GPU is a rendered
2	pixel count regis	ter.	
1	3	1.	The method of claim 29, wherein the blit instruction is adapted to store
2	a control value in	n a co	ntrol register in response to the colorkey operation, and wherein the
3	control value is adapted to instruct the GPU to abort the processing of the second set of		
4	rendering commands.		
1	32	2.	The method of claim 31, wherein the control value is a clip plane
2	distance.		
1	3:	3.	An information storage medium having a set of instructions adapted to
2	direct an information processing device in communication with a graphics processing unit		
3	(GPU) to perform the steps of:		
4	w	riting	a first set of rendering commands to a command buffer;
5	w	riting	a set of self-programming commands including a blit instruction to the
6	command buffer	; and	
7	w	riting	a second set of rendering commands to the command buffer.
1	34	4.	The information storage medium of claim 33, wherein the first set of
2	rendering commands, the set of self-programming commands, and the second set of rendering		
3	commands are w	ritten	sequentially to the command buffer.
1	3:	5.	The information storage medium of claim 33, wherein the first set of
2	rendering comm	ands i	is associated with a first image to be rendered to a first display buffer,
3	the second set of rendering commands is associated with a second image to be rendered to a		
4	second display buffer, and the set of self-programming commands is adapted to instruct the		
5	GPU to display t	the fir	st image.
1	3	6.	The information storage medium of claim 35, wherein the blit
2	instruction is ada	apted	to store a memory address associated with the first display buffer in a
3	control register of	of the	GPU.

37. The information storage medium of claim 33, wherein the first set of		
rendering commands is associated with a bounding box associated with an object and the		
second set of rendering commands is associated with the object; and further wherein the set		
of self-programming commands is adapted to instruct the GPU to evaluate the visibility of the		
bounding box and to optionally bypass the rendering of the object in response to the		
evaluation of the visibility of the bounding box.		

- 1 38. The information storage medium of claim 37, wherein the blit 2 instruction includes a colorkey operation on a register of the GPU.
- 1 39. The information storage medium of claim 38, wherein the register of the GPU is a rendered pixel count register.
- 1 40. The information storage medium of claim 38, wherein the blit 2 instruction is adapted to store a control value in a control register in response to the colorkey 3 operation, and wherein the control value is adapted to instruct the GPU to abort the 4 processing of the second set of rendering commands.
- 1 41. The information storage medium of claim 40, wherein the control value is a clip plane distance.